AMENDMENTS TO THE CLAIMS

Please add new claims 10-19 in accordance with the following list of claims:

1. (Original) A semiconductor memory device comprising:

a plurality of memory banks each including a memory cell array and a control circuit for the memory cell array; and

an interface circuit shared by the plural memory banks;

the semiconductor memory device being adapted for performing reading of data from the plural memory banks and rewriting of data to the plural memory banks,

wherein in an operation mode for performing the reading, the following processing is performed:

processing A1 in which the interface circuit outputs an active read enable signal to the plural memory banks;

processing A2 in which the interface circuit outputs address information specifying a memory cell as a reading target to the plural memory banks;

processing A3 in which each of the plural memory banks reads out data of the memory cell specified by the inputted address information and outputs the read-out data as an output data group to the interface circuit; and

processing A4 in which the interface circuit selectively outputs one of plural output data groups outputted from the plural memory banks, to outside, and

in an operation mode for performing the rewriting, the following processing is performed:

processing B1 in which the interface circuit outputs address information specifying a memory cell as a rewriting target to the plural memory banks;

processing B2 in which the interface circuit outputs an input data group from outside to the plural memory banks;

processing B3 in which the interface circuit selectively outputs an active write enable signal to one of the plural memory banks; and

processing B4 in which a memory bank to which an active write enable signal is inputted, of the plural memory banks, rewrites data of the memory cell specified by the address information to data of the input data group.

2. (Original) The semiconductor memory device as claimed in claim 1, wherein the memory bank to which an active write enable signal is inputted, of the plural memory banks, outputs a busy signal indicating that it is performing the processing B4.

3. (Original) The semiconductor memory device as claimed in claim 2, wherein the interface circuit does not activate the write enable signal during a period when a busy signal is received from at least one of the plural memory banks.

4. (Original) The semiconductor memory device as claimed in claim 2, wherein even during a period when a busy signal is received from at least one of the plural memory banks, the interface circuit outputs an active write enable signal to a memory bank that is not outputting a busy signal.

5. (Original) The semiconductor memory device as claimed in claim 1, wherein in a test mode for the plural memory banks, the following processing is performed:

processing C1 in which the interface circuit outputs address information specifying a memory cell as a rewriting target to the plural memory banks;

processing C2 in which the interface circuit outputs an input data group from outside to the plural memory banks;

processing C3 in which the interface circuit outputs an active write enable signal to the plural memory banks; and

processing C4 in which the plural memory banks rewrite data of the memory cell specified by the address information to data of the input data group.

6. (Original) The semiconductor memory device as claimed in claim 2, wherein in a test mode for the plural memory banks, the following processing is performed:

processing D1 in which the interface circuit outputs address information specifying a memory cell as a rewriting target to the plural memory banks;

processing D2 in which the interface circuit outputs an input data group from outside to the plural memory banks; and

processing D3 in which the interface circuit outputs an active write enable signal to one of the plural memory banks; and

wherein the memory bank to which an active write enable signal is inputted, of the plural memory banks, rewrites data of the memory cell specified by the address information to data of the input data group, and

even during a period when a busy signal is received from at least one of the plural memory banks, the interface circuit outputs an active write enable signal to a memory bank that is not outputting a busy signal.

7. (Original) The semiconductor memory device as claimed in claim 1, wherein the interface circuit comprises:

an interface core block for outputting a bank address for selecting one of the plural memory banks;

a selector element for selecting and outputting one of plural output data groups outputted from the plural memory banks on the basis of the bank address in the operation mode for performing the reading; and

a write enable signal control circuit for selecting one of the plural memory banks on the basis of the bank address and outputting an active write enable signal to the selected bank memory in the operation mode for performing the rewriting;

the processing A1, A2, B1 and B2 being performed by the interface core block;

the processing A3 being performed by the selector element;

the processing B3 being performed by the write enable signal control circuit.

8. (Original) The semiconductor memory device as claimed in claim 5, wherein the interface circuit comprises:

an interface core block for outputting a bank address for selecting one of the plural memory banks;

a selector element for selecting and outputting one of plural output data groups outputted from the plural memory banks on the basis of the bank address in the operation mode for performing the reading; and

a write enable signal control circuit for selecting one of the plural memory banks on the basis of the bank address and outputting an active write enable signal to the selected bank memory in the operation mode for performing the rewriting;

the processing A1, A2, B1, B2, C1 and C2 being performed by the interface core block;

the processing A3 being performed by the selector element;

the processing B3 and C3 being performed by the write enable signal control circuit.

9. (Original) The semiconductor memory device as claimed in claim 6, wherein the interface circuit comprises:

an interface core block for outputting a bank address for selecting one of the plural memory banks;

a selector element for selecting and outputting one of plural output data groups outputted from the plural memory banks on the basis of the bank address in the operation mode for performing the reading; and

a write enable signal control circuit for selecting one of the plural memory banks on the basis of the bank address and outputting an active write enable signal to the selected bank memory in the operation mode for performing the rewriting;

the processing A1, A2, B1, B2, D1 and D2 being performed by the interface core block;

the processing A3 being performed by the selector element;

the processing B3 and D3 being performed by the write enable signal control circuit.

10. (New) A semiconductor memory device comprising:

a plurality of memory banks each of which is controlled by a read enable signal and a write enable signal, the memory banks providing output data and a plurality of busy signals, respectively; and

an interface circuit connected to the memory banks, the interface circuit including:

an interface core block connected to the memory banks, the interface core block providing the read enable signal to the memory banks, the write enable signal and a bank address;

a write enable signal control circuit connected to the memory banks and the interface core block, the write enable signal control circuit providing a plurality of secondary write enable signals to the memory banks, respectively, in response to the write enable signal and the bank address;

a first select circuit connected to the memory banks and the interface core block, the first select circuit selectively supplying one of the busy signals In response to the bank address; and

a second select circuit connected to the memory banks and the interface core block, the second select circuit selectively supplying the output data in response to the bank address.

11. (New) A semiconductor memory device according to claim 10, wherein each of the memory banks comprises:

a control circuit connected to the interface core block and the second select circuit, the control circuit receiving the write enable signal and providing one of the busy signals; and

a plurality of memory cells for providing the output data to the second select circuit.

12. (New) A semiconductor memory device according to claim 10, wherein the write enable signal control circuit includes a plurality of inverters and a plurality of NOR circuits.

13. (New) A semiconductor memory device according to claim 10, wherein the interface core block provides a test signal to the write enable signal control circuit, and wherein the write enable signal control circuit provides the secondary write enable signals to the memory banks, respectively, in response to the write enable signal, the test signal and the bank address.

14. (New) A semiconductor memory device according to claim 13, wherein the write enable signal control circuit includes a plurality of inverters and a plurality of NOR circuits.

15. (New) A semiconductor memory device comprising:

a plurality of memory banks each of which is controlled by a read enable signal and a write enable signal, the memory banks providing output data and a plurality of busy signals, respectively; and

an interface circuit connected to the memory banks, the interface circuit including:

an interface core block connected to the memory banks, the interface core block providing the read enable signal to the memory banks, the write enable signal and a bank address;

a write enable signal control circuit connected to the memory banks and the interface core block, the write enable signal control circuit providing a plurality of secondary write enable signals to the memory banks, respectively, in response to the write enable signal and the bank address;

a busy signal control circuit connected to the memory banks and the interface core block, the busy signal control circuit supplying a control signal in response to the busy signals; and

a select circuit connected to the memory banks and the interface core block, the select circuit selectively supplying the output data in response to the bank address.

16. (New) A semiconductor memory device according to claim 15, wherein each of the memory banks comprises:

a control circuit connected to the interface core block and the busy signal control circuit, the control circuit receiving the write enable signal and providing one of the busy signals; and

a plurality of memory cells for providing the output data to the select circuit.

17. (New) A semiconductor memory device according to claim 15, wherein the write enable signal control circuit includes a plurality of inverters and a plurality of NOR circuits.

18. (New) A semiconductor memory device according to claim 15, wherein the interface core block provides a test signal to the write enable control circuit, and wherein the write

enable signal control circuit provides the secondary write enable signals to the memory banks, respectively, in response to the write enable signal, the test signal and the bank address.

19. (New) A semiconductor memory device according to claim 18, wherein the write enable signal control circuit includes a plurality of inverters and a plurality of NOR circuits.